In the Claims

Please amend the claims and add new claims as indicated below. This listing of claims replaces all prior versions.

1. (currently amended) A memory system that receives addresses corresponding to data in an order comprising:

an address buffer that receives addresses in said order;

a memory array;

a control circuit that selects ~~at a given cycle~~ a memory reference from a set of pending memory references in said address buffer to present to the memory array, said references being presented to said memory array ~~as they leave the control circuit~~ in an order different than the order in which they were received; and

a read buffer, that receives data read out from the memory array.

2. (currently amended) A memory system according to claim 1, wherein said control circuit causes the read buffer to read out data from the ~~read buffer~~ memory array in said order as received by the address buffer ~~with respect to read requests~~.

3. (original) A memory system according to claim 1 wherein the control circuit performs multiple accesses in sequential cycles to a given row in the memory in the order in which the addresses corresponding to the given row were received.

4. (original) A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs multiple accesses in sequential cycles to an active row of a given bank before activating a different row of the given bank.

5. (original) A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs multiple accesses in sequential cycles to an active row of a given bank before activating a different bank.

6. (original) A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs a row access to a currently inactive bank when another bank contains a currently active row.

7. (original) A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks and the address buffer is partitioned into a separate address buffer for each bank.

8. (currently amended) A memory system according to claim 1 wherein said control circuit comprises:

a comparator ~~for each address capable of being stored in the address buffer~~ which compares the row address of each address stored in the address buffer with the row address of ~~the~~ a currently active row of said memory array; and

a priority encoder that selects the first address entered into the address buffer that corresponds to ~~is contained in~~ the currently active row of the memory array.

9. (original) A memory system according to claim 1, wherein, associated with the read buffer is a head pointer and a tail pointer to assist in tracking the order sequence of read access requests, and a buffer array containing a status flag for each read access request having an associated address currently stored in the address buffer.

10. (currently amended) A memory system according to claim 1 wherein, during each of a plurality of sequential cycles, the address buffer ~~inputs~~ receives a new address and the control circuit compares the new address to the address of the currently active row in the memory array.

11. (currently amended) A memory system according to claim 7 wherein, during each of a plurality of sequential cycles, the address buffer ~~inputs~~ receives a new address and the control circuit compares the new address to the address of the currently active

row of the memory array if the currently active row is in the same bank as the new address.

12. (currently amended) A memory system according to claim 11 wherein, if ~~the address buffer inputs the new address and~~ the new address does not correspond to the same bank as the address of the currently active row, the control circuit does not perform a comparison of the new address to the address of the currently active row.

13. (currently amended) A method of accessing memory having a state of data accessibility that changes in response to data accessed in the memory, the method comprising ~~the steps of~~:

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receiving a ~~sequential~~ plurality of memory access requests in a first order ~~the form of an address inputs~~;

buffering the plurality of ~~address inputs~~ memory access requests;

initiating an out of order memory access request to a memory array for one of the ~~sequential~~ plurality of memory access requests such that at least one of the plurality of memory access requests ~~address inputs is requested~~ is presented in another order different than the first order ~~in which the one address was received~~; and

~~selecting at a given cycle a memory reference from among a set of pending memory references and presenting this memory reference to said memory array; and~~

buffering read results ~~of those memory access requests~~ corresponding to the received memory access requests ~~read operations~~.

14. (currently amended) A method according to claim 13 wherein ~~said step of~~ initiating ~~initiates~~ the out of order memory access ~~initiates said request to an address having a row corresponding to a currently active row~~ occurs as a function of the state of the memory before the received memory access requests are used to access the memory, and wherein the state of the memory is at least partly defined as a function of data-access speed for a segment of data stored in the memory.

15. (currently amended) A method according to claim 13 ~~wherein the buffered read results are read out in the in the order that the original read requests were made~~ further including receiving another memory access request before receiving a plurality of memory access requests in a first order, and wherein initiating occurs after receiving the other memory access request.

16. (currently amended) A method according to claim 13 wherein ~~multiple accesses in sequential cycles to a given row in the memory array are made in the order in which the addresses corresponding to the given row were received~~ a plurality of addresses are accessed in a currently active segment of the memory in said second order different from said first order and before another segment of the memory is made currently active.

17. (currently amended) A method according to claim 13 wherein a plurality of addresses are accessed ~~row accesses are performed out of order to a currently active row~~ in a currently active row in said second order different from said first order and before another row is made currently active.

18. (currently amended) A method according to claim 13 wherein the memory ~~array~~ is partitioned into a plurality of banks, and a row access is performed on a row of a currently inactive bank when another bank contains a currently active row.

19. (currently amended) A method according to claim 13 wherein ~~the step of~~ buffering read results includes setting a read tail pointer to identify a next sequential location ~~of~~ in a buffer and setting a read head pointer to remove data from the buffer.

20. (new) A memory system that receives addresses corresponding to data, comprising:

an address buffer that receives addresses in a first order;

a memory array; and

control means for prioritizing the received addresses as a function of data-access efficiency before the received addresses are used to access the memory array, and for using the received addresses to access the memory array, the memory array data being accessed in a second order that is different from the first order.

21. (new) For use in a memory system having a memory array that stores data corresponding to addresses, a method for accessing the data comprising:

receiving the addresses in a first order; and

prioritizing the received addresses as a function of data-access efficiency before the received addresses are used to access the memory array, and using the received addresses to access the memory array, the memory array data being accessed in a second order that is different from the first order.

22. (new) The method of claim 21, further including tracking states of accessibility for the stored data in response to accesses to the memory array, and wherein prioritizing the received addresses provides data access that is faster than would be provided by the first order.

23. (new) A memory system that receives addresses corresponding to data, comprising:

an address buffer that receives addresses in a first order;

a memory array; and

a control circuit adapted to prioritize the received addresses as a function of data-access efficiency before the received addresses are used to access the memory array, and then to use the received addresses to access the memory array, the memory array data being accessed in a second order that is different from the first order.

24. (new) The memory system of claim 23, further including a read buffer communicatively coupled to the control circuit and adapted to reorder, according to the first order of received addresses, data accessed from the memory array.

25. (new) The memory system of claim 23, wherein the second order is established to provide data access that is faster than would be provided by the first order.

26. (new) The memory system of claim 23, wherein the control circuit is further adapted to establish the second order within the address buffer, and the address buffer is adapted to use the second order to access the memory array.

27. (new) A memory system that receives addresses corresponding to data, comprising:

an address buffer adapted to receive addresses in a first order;

a memory array storing data corresponding to the received addresses; and

a control circuit adapted to reorder the received addresses as a function of data-access efficiency and cause the address buffer to access the corresponding data stored in the memory array according to the reordering of the received addresses.

28. (new) The memory system of claim 27, further including a read buffer communicatively coupled to the control circuit and adapted to reverse the reordering of the received addresses.

29. (new) The memory system of claim 27, wherein the reordering is established to provide data access that is faster than would be provided by the first order.

30. (new) The memory system of claim 27, wherein the control circuit is further adapted to track states of accessibility for the stored data in response to accesses to the memory array, and wherein reordering is established to provide data access that is faster than would be provided by the first order.

31. (new) A memory system that receives addresses corresponding to data in an order comprising:

an address buffer that receives addresses in said order;

a memory array having data with respective states of accessibility that change in response to accesses to the memory array;

a control circuit that selects, as a function of the state of the memory array before the received addresses are used to access the memory array, a memory reference from a set of pending memory references in said address buffer to present to the memory array, said references being presented to said memory array in an order different than the order in which they were received; and

a read buffer, that receives data read out from the memory array.